RF Up/Down Conversion Is Simplified By Linear Arrays

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Linear Arrays Have Advantages Over Discrete Transistors

Discrete transistors have been used to build RF up/down converters in the past because they were the only cost effective technology available. Linear semiconductor process improvements have increased the frequency response of ICs to the point where liner arrays are rapidly replacing discrete devices. Linear arrays are a group of transistors made with an IC process, and there can be both NPN and PNP transistors on one piece of silicon. The linear array is usually packaged in a PDIP or SOIC case, but the next generation arrays will be packaged in a SOT36 outline as well.

Discrete transistors are hard to use because each transistor is expensive and space consuming, so the design becomes an art of utilizing each transistor to its maximum limit, an art which can take years to master. Single transistor designs, see Figure 1, predominate in low cost equipment where the design requirements are not very severe. More transistors are required to meet the demanding specifications imposed by higher cost equipment, because each transistor is limited in the power gain it can supply. Also, all of the transistors must have a bias circuit which usually includes negative feedback for DC stability. Some gain is lost because of this bias circuitry, so multistage transistor designs are required for all but the simplest requirements.

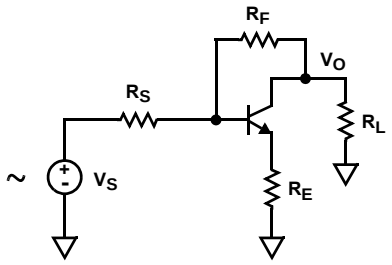

FIGURE 1. DISCRETE TRANSISTOR AMPLIFIER

The multistage transistor amplifier design shown in Figure 2 uses Q_4 and Q_5 for bias stability, while Q_2 does the amplification. This circuit nearly achieves the maximum transistor gain because the bias stability is achieved through transistor matching rather than negative feedback. This highlights another shortcoming of discrete transistor designs which is their lack of matching characteristics. Without matching most of the advantage gained by the amplifier shown in Figure 2 is lost. After the first transistor is paid for in a linear array, additional transistors cost little because they take little space on the same piece of silicon. This multistage circuit configurations can be employed with linear arrays at a small additional cost. Many transistors, some resistors, and sometimes capacitors can be included on the same piece of silicon thus further easing multistage circuit design.

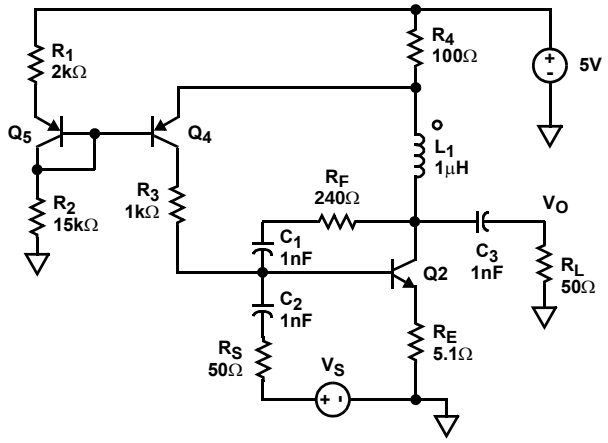

FIGURE 2. MULTISTAGE TRANSISTOR AMPLIFIER

The advantages of linear arrays over discrete transistors are less components, increased reliability, decreased incoming test time, lower cost, and better circuit performance. Discrete transistors retain one advantage over linear arrays because they can be fabricated for very special performance characteristics such as super high frequency response or high breakdown voltage.

What Comprises A Linear Array

The two first items which are considered when designing a linear array are what semiconductor process and what package will be used. The process determines the parameters such as frequency response, gain, and breakdown voltage that the transistors in the linear array will have. The package determines the size of the linear array die and the number of leads (bond pads), hence it ultimately determines the number of transistors which can be put in the array.

The types of devices and how they will be bonded out are determined by product marketing. If the array is to be general purpose it will contain a block of NPN bipolar transistors, a block of PNP bipolar transistors, maybe some FET transistors if the process allows, and possibly some passive devices.

Figure 3 shows the layout diagram for the basic die which is used to make the HFA3xxx series of linear arrays. Notice that there is a block of 15 NPN bipolar transistors, a block of 11 PNP bipolar transistors, and a block of 4 FET transistors. The process used to make the HFA3xxx die yields NPN transistors with an f_t of 9GHz and PNP transistors with an f_t of 5.5GHz. The parameter f_t is a measure of the transistor's high frequency performance, and it is often unsymmetrical (NPN vs PNP) as shown here. There are two metal layers with interconnections which can be used to connect the transistors contained in the HFA3xxx die into various circuit configurations.

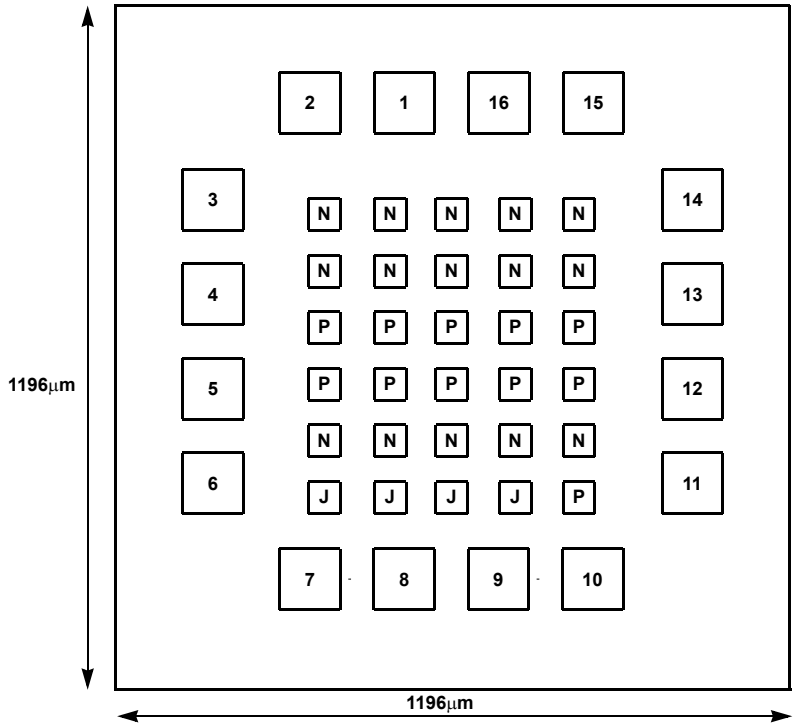

FIGURE 3. LAYOUT DIAGRAM FOR THE HFA3XXX LINEAR ARRAYS

Four different linear arrays are made from the same base HFA3xxx die by using the metal masks to connect different transistors to the bonding pads. These linear arrays, shown in Figure 4, are the HFA3046 and the HFA3127 linear arrays which contain all NPN transistors, the HFA3128 which contains all PNP transistors, and the HFA3096 which contains a mix of NPN and PNP transistors. These linear arrays have been available for design since 1993, and the multistage amplifier shown in Figure 2 is made from the HFA3096.

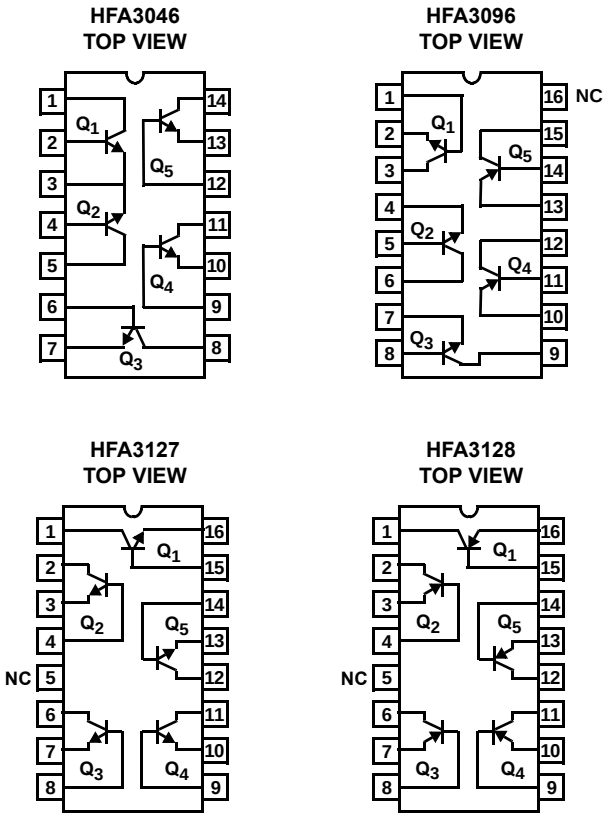

FIGURE 4. CIRCUIT DIAGRAMS FOR THE HFA3046, HFA3096, HFA3127 AND HFA3128

Figure 5 shows the HFA3101 and HFA3102 linear array schematics, both which have been made from the HFA3xxx die. The HFA3102 is a dual-long tailed transistor pair; a configuration often used to make voltage controlled gain and differential amplifier circuits. The HFA3101 is configured as a Gilbert cell which is often used for multipliers.

Discussion of the HFA3101 Gilbert Cell

The metallization diagram for the HFA3101 is shown in Figure 6. The HFA3101 is a very versatile RF building block, which has been carefully laid out to improve its matching properties. Notice that the layout is as symmetrical as possible which minimizes distortion due to area mismatches, thermals, betas, and ohmic resistance. The symmetry insures that both long tailed pairs will track when the IC is subjected to temperature or stress, and consequently the whole cell will remain stable.

HFA3101

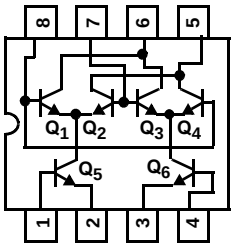

FIGURE 5A. GILBERT CELL

HFA3102

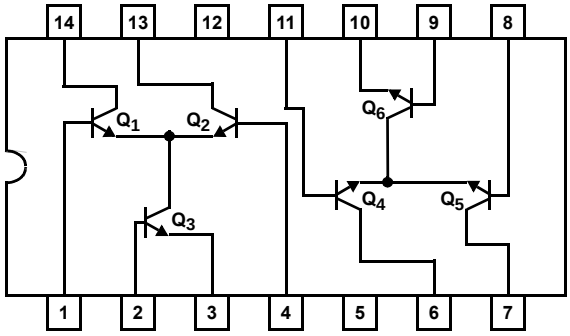

FIGURE 5B. DUAL LONG-TAILED TRANSISTOR PAIR

FIGURE 5. COMPLEX CIRCUITS MADE FROM LINEAR ARRAYS

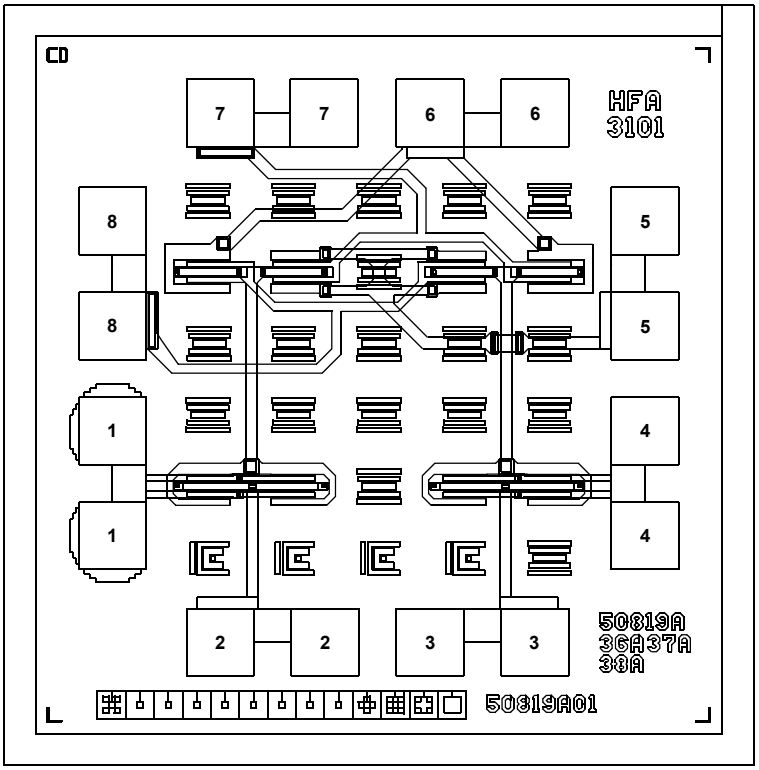

FIGURE 6. METALLIZATION MASK LAYOUT DIAGRAM FOR THE HFA3101

The cell is made from two long-tailed pair stages built as two variable transconductance multipliers in parallel with their outputs cross coupled. This configuration is known in the industry as a Gilbert cell (see Figure 5A), and it enables four quadrant multiplier operation. The cell has restricted use as a linear four quadrant multiplier because there are input dynamic range restrictions for the upper differential pair and lower tail transistors. The input range restrictions are confined to the input signal levels, thus this configuration is quasi-confined to applications where it's linear response is only required at one input. Such as in modulator or mixer circuits. Up converters, down converters, frequency doublers, and frequency/phase detectors often use this configuration with great success. Emitter degeneration, gained by adding an external emitter resister, improves the dynamic range and linearity, so the lower pair emitters have been brought out to leads for this purpose.

The upper quad transistors are used as switches in modulator applications (see Figure 5A). Q_1/Q_2 and Q_3/Q_4 are used as on/off switches so they do not saturate, consequently the modulator will have a very high frequency response. The upper switches are controlled by the carrier input signal, while the modulating signal is applied to the lower tail transistors, Q_5/Q_6. If the modulation is to be linear, the modulating signal must be significantly below the threshold voltage of 26mV to keep the lower tail transistors in their linear region. Higher input modulating signals can be handled by adding an emitter degeneration resistor. The waveforms for the modulator are shown in Figure 7.

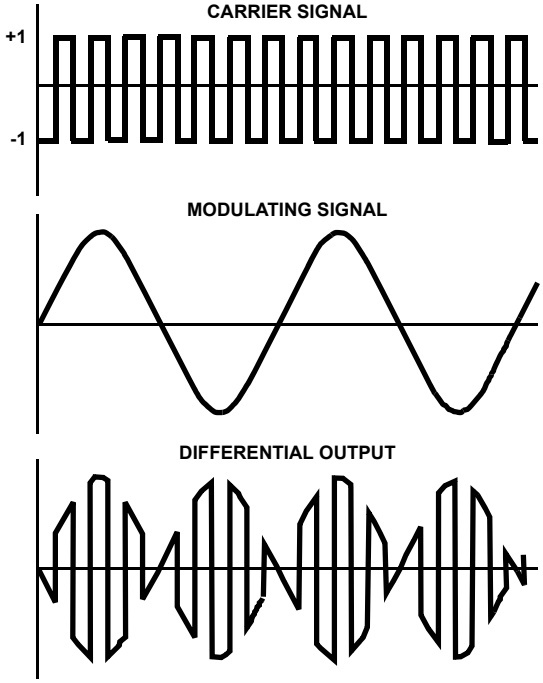

FIGURE 7. MODULATOR INPUT/OUTPUT SIGNALS

When the upper quad and lower tail transistors are both operated in their linear region the cell functions as a linear multiplier. If the carrier frequency, f_C, and the modulating frequency, f_M, are put into the different inputs they will be multiplied together by the equation $f_{AM} = f_C +,-f_M$. The circuits which perform this function are called mixers, and the result is known as AM modulation as shown in Figure 8.

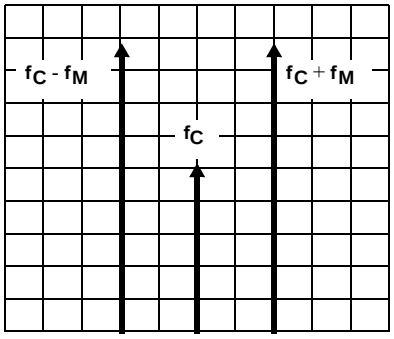

FIGURE 8A. UP CONVERSION OR SUPPRESSED CARRIER AM

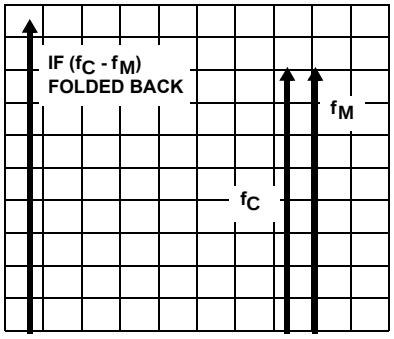

FIGURE 8B. DOWN CONVERSION

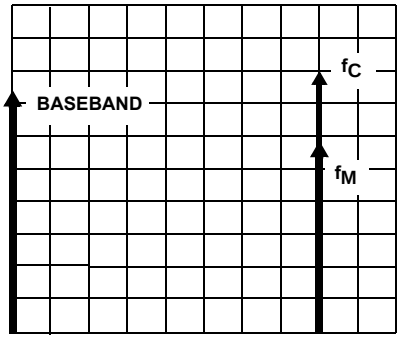

FIGURE 8C. ZERO IF OR DIRECT DOWN CONVERSION

FIGURE 8. AM MODULATION WITH A GILBERT CELL

Downconverter and Upconverter Design

This section describes the design of a downconverter shown in Figure 9, and an upconverter shown in Figure 10. Both converters operate in the 900MHz frequency range, and both are powered from a three volt power supply. The heart of the both converters is the Gilbert cell linear array, and the local oscillator signal will always be connected to the bases of the upper quad pairs, Q_1 through Q_4. Also, the RF signal for the downconverter and the modulating signal for the upconverter are applied to the base of the lower tail transistor, Q_6. Essentially the circuits are the same because they perform the same multiplication function in the same manner with the same transistors; the major difference is the output coupling networks which act as filters to select the output signal.

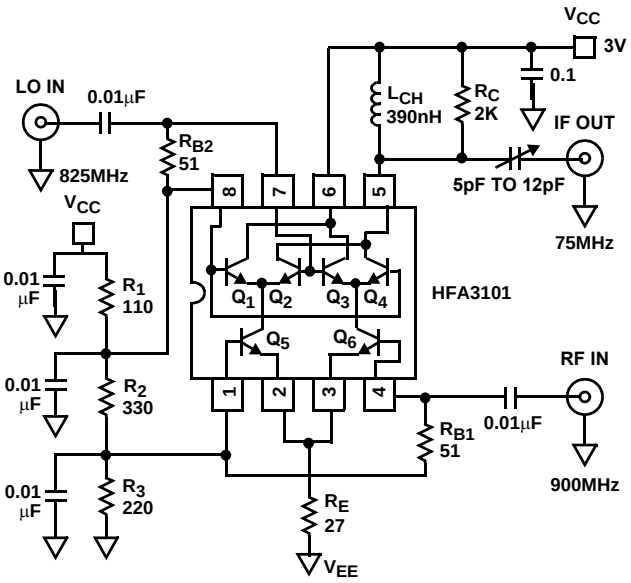

FIGURE 9. 3V DOWN CONVERTER APPLICATION

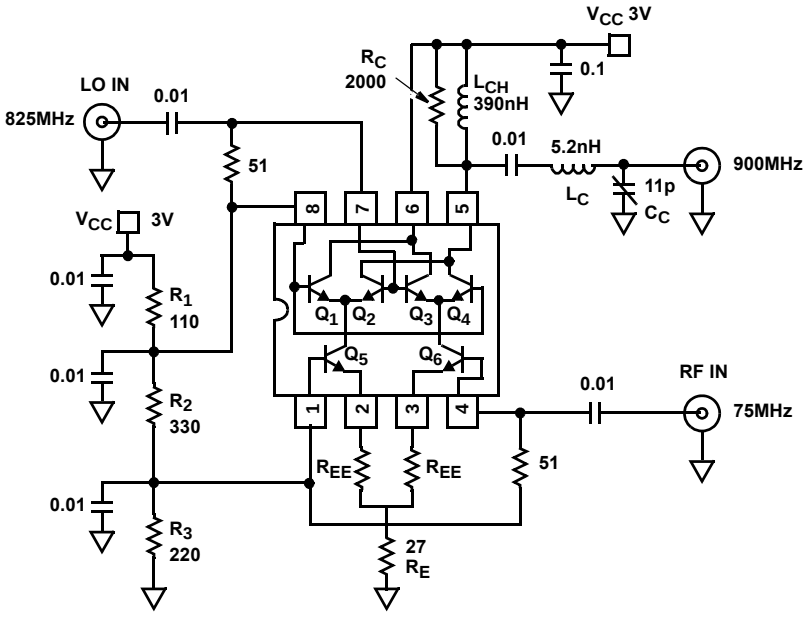

FIGURE 10. 3V UP CONVERTER APPLICATION

Summary

Linear arrays are comprised of many transistors, NPN, PNP or a combination on a single die. Because putting all of the transistors on the same die gains excellent matching characteristics and reduces cost, the design of multistage high frequency circuits is simplified. The manufacturers utilize the base die to make many different linear arrays. Linear arrays and their spin-offs such as the HFA3101 Gilbert cell enable the fast and efficient design of many different low and high frequency circuits such as up and down converters. This linear array offers the designer flexibility, lower cost, improved reliability, and improved performance. They are powerful RF building blocks.